REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier. No Claims are currently being amended. Claims 19-38 remain pending in this application.

Claims 21-24 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,976,930 (Noble). The Examiner states:

> Referring to figures 2a-3, Noble teaches an integrated circuit including at least one transistor, the integrated circuit comprising:
>
> a pair of local interconnects (200) spaced from each other, and
>
> a gate of the transistor (170/161/162) disposed in the space between the local interconnects (200) and separated from of the local interconnects by an insulating liner (190),

Applicants respectfully traverse the rejection.

Claim 21 explicitly recites that the gate of the transistor is disposed in the space between the local interconnects. The disposition of the gate between the local interconnects provides significant advantages for integrated circuit fabrication. This disposition is not accounted for in the Examiner's rejection.

The Examiner's rejection refers to polysilicon structures (200) of Noble as the local interconnects. However, gate (139) of Noble is not provided in the space between structures (200). Word lines (162) of Noble are provided in the space between polysilicon structures (200). Word lines (162) are not gates. Gate (139) is provided between contacts (140) and (142). See, Figure 3 of the Noble. In fact, gate (139) appears to be bigger than the space between polysilicon

structures (200). Accordingly, claim 21 and its dependent claims 22-24 are patentable over the cited art.

On page 3 of the Office Action, claims 19-24 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,005,272 (Gardner). The Examiner states:

> Gardner et al. teaches an integrated circuit including at least one transistor, the integrated circuit comprising:
>
> a pair of local interconnects (138a/138b) spaced from each other by a minimum lithographic feature and each being a minimum lithographic feature (see col. 5, lines 28-31); and
>
> a gate of the transistor (134/144) disposed in the space between the local interconnects and separated from of the local interconnects by an insulating liner (150a/150b), wherein the space in less than or equal to the minimum lithographic feature, whereby the width of the transistor is not greater than three of the minimum lithographic feature (see figures 1a-1t, see col. 5, lines 28-31).
>
> Regarding to claim 20, wherein the insulating liner (150a/150b) are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate (see figures 1P).
>
> Regarding to claim 22, the pair of local interconnect are space from each other by a minimum lithographic feature (see figures 1k, see col. 5, lines 28-31).
>
> Regarding to claim 23, the insulating liners (150a/150b/150c) are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate (see figures 1P).
>
> Regarding to claim 24, a source and drain (138a/138b) are disposed by at least partially beneath the insulating liner (150a/150b/150c, see figure 1R).

Applicants respectfully traverse the rejection.

The rejection of claims 19-24 is improper for at least two reasons. Both independent claim 19 and claim 21 recite that the gate is disposed in the space between the local

interconnects. This recitation requires two structures which are not addressed in the Examiner's rejection based upon Gardner.

First, Gardner does not anticipate claims 19-24 for a similar reason to that discussed above with respect to Noble. Gate (144) in Gardner is not disposed in a space between regions (134a/134b). Indeed, the space between regions (134a/134b) is the channel region for the transistor. Gate (144) is disposed above regions (138a/138b) and indeed is even larger than the space between regions (138a/138b).

Second, drain and source regions (138a/138b) are referred to as local interconnects in the rejection. However, regions (138a/138b) are not local interconnects, but are rather source and drain regions. See, col. 8, lines 24-46. Source and drain regions (138a/138b) of Gardner serve an entirely different purpose than local interconnects and are simply not local interconnects.

Accordingly, the rejection based upon Gardner does not account for each and every limitation in independent claim 19 and 21. Accordingly, claim 19 and its dependent claim 20 and independent claim 21 and its dependent claims 22-24 are patentable under Gardner because at least two limitations are missing from the Examiner's rejection based upon Gardner.

On page 4 of the Office Action, claims 19-24 are rejected as being unpatentable over U.S. Patent No. 5,583,355 (Bernhardt). The Examiner states:

> Bernhardt et al teaches an integrated circuit including at least one transistor, the integrated circuit comprising:
>
> a pair of local interconnects (26a/26b) spaced from each other by a minimum lithographic feature and each being a minimum lithographic . . .
>
> Therefore , it would have been obvious to an ordinary skill in the requisite art at the time of the invention was made would form a transistor wherein the width is not greater than three minimum lithographic feature because forming a transistor wherein the width is not greater than three minimum lithographic feature would provide more high density on the chip.

Applicants respectfully traverse the rejection.

With respect to independent claim 19, claim 19 recites two specific dimensional limitations that are not shown, described or suggested in Bernhardt. Claim 19 recites that the transistor width is less than or equal to three minimum lithographic features and that the local interconnects each have a width of one lithographic feature. These two dimensional aspects of claim 19 provide significant advantages in the formation of integrated circuits.

Bernhardt fails to disclose or suggest that the width of the transistor is not greater than three lithographic features and that the local interconnects are one lithographic feature. In direct contrast to the structure recited in independent claim 19, Bernhardt appears to disclose that the lithographic feature is the width of gate (16). See, col. 2, lines 45-48. Accordingly, the width of the transistor is substantially more than three lithographic features and each of the contacts (32a) and (32b) has a width greater than one lithographic feature. This type of design is completely ignorant of the advantages associated with the present invention as recited in claim 19.

The structure of claim 19 minimizes transistor size by providing local interconnects having a width of a lithographic feature and placing a gate within a space between the local interconnects, thereby achieving a total width of three minimum lithographic features or less. There is nothing in Bernhardt that provides a motivation to utilize such a structure. Indeed, the mere fact that Bernhardt utilizes a conventional process which forms gate (16) first and the contacts (33) after the gate is formed indicates that it has no contemplation of the advantages associated with this structure of claims 19. Accordingly, independent claim 19 and its dependent claim 20 is patentable over Bernhardt.

With respect to independent claim 21, independent claim 21 recites that the gate and an insulating liner are disposed in a space that is one lithographic feature wide. Accordingly, the gate is less than one lithographic feature wide because the gate and the liner both occupy the one lithographic feature width of the space.

As discussed above with respect to independent claim 19, Bernhardt does not disclose or suggest a gate having a width less than one lithographic feature. In direct contrast to the structure recited in independent claim 21, Bernhardt appears to disclose that the lithographic feature is the width of gate (16). See, col. 2, lines 45-48. Accordingly, claim 21 and its dependent claims 22-24 are patentable over Bernhardt.

On page 6 of the Office Action, claims 25-38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,940,710 (Chung) in view of U.S. Patent No. 5,955,768 (Liaw). The Examiner states:

> Referring to fig. 2a-2e, Chung et al. teaches an integrated circuit including at least a pair of local interconnects with one interconnect on each side of gate transistor, the integrated circuit being manufactured by a method comprising the steps of:
>
> forming on a semiconductor substrate (1) a thick insulating layer (6);
>
> forming at least a pair of space apart openings (30) and the drain (14) in one of the openings;
>
> filling each of the openings with a conductive material (8) to form the local interconnects (8), the local interconnect being electrically couple to the source and drain (14);
>
> removing a portion of the insulating layer (6) to forma gate opening between the local interconnects (8);
>
> forming a gate dielectric (4) on the semiconductor substrate (1) in the gate opening; and
>
> forming the gate (5) on the gate dielectric layer.
>
> With regard to claims 25-26, 28-31, the terms "forming", "filling", "removing", "etch selectively relative to" is method recitations in device claimed, and they are non-limiting, because only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113 Moreover, an old or obvious

product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding to claim 27, see figure 2d.

Regarding claim 32, see figure 2e.

Regarding to claim 33, see figure 2e, col. 6, and lines 10-11.

Regarding to claims 37-38, the term "etching stop layer is formed on semiconductor substrate before forming the thick insulating layer" and "the etching selectively" is method recitations in a device claimed, and they are non-limiting, because only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Chung et al. teaches all of the limitations as described in the claimed invention above. However, Chung et al. does not teach or suggested an etching stop layer, and forming barrier layer Titanium nitride before forming conductive material tungsten.

Liaw et al. teaches forming an etching stop layer (40, silicon nitride) before forming the thick insulating layer (ILD), forming a barrier layer titanium nitride (42) in the opening (W4/W5) and forming a conductive material tungsten (PL2/PL3).

Applicants respectfully traverse the rejection.

Claim 25 recites a particular method which inherently causes the transistor to have particular structure. For example, claim 25 recites removing a portion of the insulating layer to form a gate opening between the local interconnects. This technique allows a smaller transistor having a relatively small width compared with lithographic feature sizes to be formed.

Chung and Liaw disclose a very different structure. Chung shows a conventional process in which the gate is formed first. Liaw fails from the exact same deficiency. There is not a suggestion in Chung or Liaw for forming the gate after the local interconnect. Accordingly, independent claim 25 and its dependent claims 16-58 are patentable over Chung and Liaw.

Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. § 1.136 and authorize payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date 2-28-05

By _____

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